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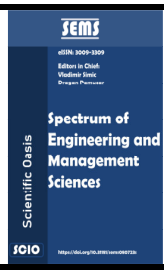

Optimized Task Deployment in Dynamic Voltage and Frequency Scaling-Enabled Network-on-Chip Systems: Enhancing Energy Efficiency and Real-Time Responsiveness

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ABSTRACT

In modern multi-design computing systems, which employ dynamic voltage and frequency scaling (DVFS) and network-on-chip (NoC) communications, the optimization of task deployment is precarious for enhancing overall system performance. It introduces a comprehensive methodology that integrates task allocation, scheduling, frequency management, redundancy handling, and diverse data routing approaches. The aim is to optimize energy intake, real-time responsiveness, and system heftiness. The system design features a primary processing element associated with three slave computing units (CUs) within a 2D mesh network, with the primary CU connected to a co-processor for dependent task scheduling. This research also proposes innovative algorithms for co-processor and real-time operating system (RTOS) scheduling to reduce latency and boost power efficiency. These methodologies aim to maximize job scheduling efficiency in RTOS environments, thus refining overall system performance.

1. Introduction

The landscape of computing has been reshaped by multicore architectures, which amalgamate numerous processors onto a solitary chip, yielding platforms characterized by diminished supply frequency, heightened data throughput, and augmented energy efficiency [1]. Recent strides in nanoscale technologies have fostered a paradigm shift towards network-on-chips (NoCs) for processor communication, supplanting traditional, non-scalable data buses [2].

The computational complexity at the processors is small in comparison to the overhead associated with inter-processor communication over NoCs [3], which includes both temporal and energy expenses [4]. The routing path and task mapping decisions determine this communication overhead [5,6]. Data transmission is required when dependent tasks are assigned to different processors, and manifold routing paths—like those found in mesh networks—introduce further complexity inside NoCs. As indicated in Figure 1, the objective of the task deployment is energy

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reduction under real-time limitations. To this end, we take into consideration both energy-oriented and time-oriented pathways as viable possibilities for data transmission. Therefore, as essential components of the task deployment process, inter-processor communication, task mapping, and routing path selection must be carefully considered to maximize overall system performance.

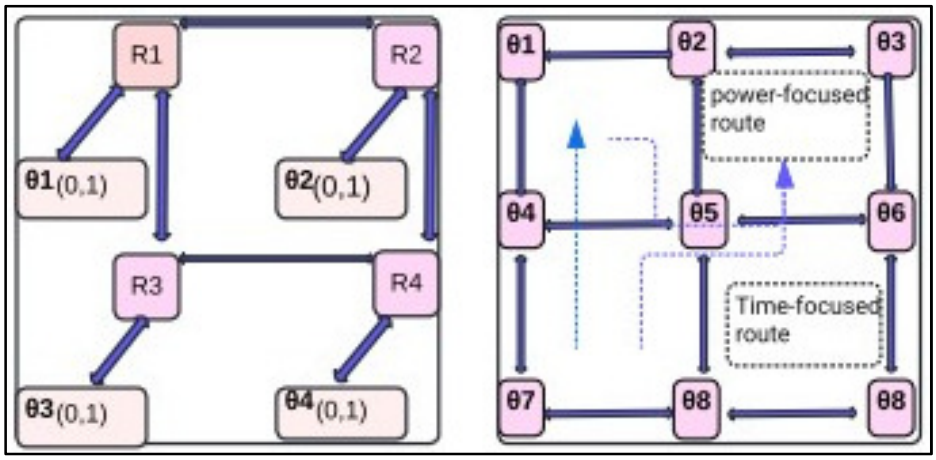

Fig. 1. NOC-based architecture

Section 2 presents a review of related literature covering power-saving techniques, offloading methodologies in RTOSs, and our specific use case. Section 3 outlines the problem statement and a proposed solution framework. Section 4 provides methodologies and techniques. The conclusion is in Section 5.

2. Literature Review

This section provides an overview of the current developments in workload distribution methods, energy conservation methods, and task assignment methodologies for multi-core systems. In an RTOS, the kernel's scheduling algorithm frequently evaluates the necessity for a context switch, selects the subsequent execution task, and manages context storage, allowing application functions to operate without synchronization, resource usage concerns, or function call ordering [7,8]. However, this approach may result in less predictable scheduling and increased system overhead, particularly in control applications.

Decentralized task distribution techniques have proven instrumental in enhancing the scheduling performance of real-time operating systems (RTOS), while concurrently, energy conservation methods strive to minimize power consumption. Employing a NoC-based multi-core system facilitates task parallelization, enabling the partitioning of applications into tasks that can be executed simultaneously across computational units. To oversee energy conservation methods, a specialized management unit dynamically monitors power usage, allocates tasks to computational units, and ensures adherence to real-time and power constraints. Table 1 categorizes representative works from the literature based on varied objectives.

Some studies have exclusively focused on offloading RTOS task scheduling onto adaptable computing platforms, neglecting the integration of energy conservation methods. Conversely, others have incorporated energy conservation methods within operating systems, with only one study [9] integrating them alongside an open-source RTOS. Notably, none of these works have explored clock gating for power optimization under the considered constraints, as delineated in Table 1.

Table 1
Comparison of task deployment

Reference	Task allocation	Multicore utilization	Optimize solution
[1]	√	√	√
[2]	✖	✖	√
[9]	√	√	√
[10]	√	√	√
[11]	√	✖	√
Proposed	√	√	√

Research indicates that offloading task scheduling from running processors can yield faster scheduling and improved predictability, reducing runtime overhead and event response time. Task scheduling can be offloaded to co-processors or hardware, with some work even replicating the entire RTOS in hardware. When dedicated kernel services such as scheduling and inter-task communication were offloaded to hardware, computing performance improved significantly. Hardware-based task scheduling markedly diminishes context switch overhead, evidenced by latency reductions.

Despite extensive research on power-saving techniques, few studies have explored their integration with RTOSs. For instance, a low-power task scheduling approach under e EDF was introduced in [12], resulting in a 27% energy conservation [13]. Similarly, a hypervisor architecture for low-power applications, dynamically adjusting operating frequency and voltage to achieve a 33% power reduction was proposed in [14]. However, these works primarily targeted Linux OS thus leaving a gap in research focusing on RTOSs and power-saving techniques.

The growing data capacity in contemporary Internet of Things (IoT) and CPS applications raises serious concerns about real-time embedded systems' memory power consumption [15]. Because real-time systems require huge memory capacities and DRAM refresh operations, memory can account for as much as 20-50% of CPU power, compared to around 10% in general-purpose systems. A novel swap mechanism is suggested to lower memory power usage to address this problem. This plan optimizes power reductions in both CPU and memory while making use of fast NVM storage. In contrast to conventional real-time task models, the task model is expanded to take storage and memory routes into consideration. This allows for the evaluation of the worst-case execution time by taking into account the overlap of CPU and memory latency.

Field programmable gate arrays (FPGAs) can be used more easily thanks to operating systems for RCOS, which abstract hardware specifics, use virtualization, and maintain shared resources [16]. They improved performance and cut down on energy usage by enabling the simultaneous execution of hardware functions on the same FPGA. Applications were able to take advantage of FPGA benefits thanks to RCOS, which also addressed issues with restricted areas and configuration port accessibility. Key ideas were explained, cutting-edge RCOS were emphasized, and future trends including real-time processing specialization, low energy consumption, dependability, safety, and security were noted.

Controlling peak power consumption is essential in contemporary multicore mixed-criticality (MC) systems to avoid thermal problems that can compromise system timeliness and dependability [17]. To minimize peak power usage during runtime, we provide an online peak power and thermal management heuristic for multicore MC systems that make use of dynamic slack and per-cluster dynamic voltage and frequency scaling (DVFS). Our method optimizes the system's peak power and temperature by choosing the best task for slack assignment. While satisfying deadline limitations in various criticality modes, experimental validation on the ODROID-XU3 platform with embedded real-

time benchmarks demonstrates up to a 5.25% decrease in system peak power and a 20.33% reduction in maximum temperature compared to existing approaches.

Multiprocessor systems-on-chips (MPSoCs) based on the NoC technology are becoming more and more common in modern embedded systems, especially for multimedia streaming applications [17]. DVFS in conjunction with task-level retiming has shown to be a successful method for dramatically lowering energy consumption in these systems. An energy-aware scheduler for real-time streaming applications in dissimilar NoC-MPSoCs is recommended in this research. R-CTG is a method that pursues to reduce retiming latency while preserving energy economy. The scheduler, ALI-EBAD, performs better in terms of energy efficiency than current job schedulers, according to experimental results.

To minimize uncertainty propagation in cloud service environments, a work proposes a unique scheduling architecture in response to these problems [19]. In this way, the architecture successfully mitigates the effects of unpredictable task execution and data transfer durations by controlling the count of workflow tasks that are directly waiting on each service instance. To dynamically modify plans in response to uncertainties, the suggested uncertainty-aware online scheduling algorithm (ROSA) combines proactive and reactive tactics. Employing simulation trials, ROSA outperforms five common algorithms, obtaining notable gains in costs (up to 56%), variance (up to 70%), resource utilization (up to 37%), and fairness (up to 37%).

A task scheduling policy that handled the coexistence of classic hard real-time jobs and sporadically arriving interactive tasks in the context of smart industrial systems integrating IoT and CPS technologies were presented in [18]. The policy is a two-phase process that used offline scheduling based on evolutionary algorithms to meet strict real-time deadlines and "virtual real-time tasks" for interactive work. Interactive tasks were scheduled online, and workloads were updated regularly to accommodate changes. According to experimental data, energy consumption might be reduced by 66.8% without compromising deadlines, allowing interactive tasks to have waiting periods of less than three seconds.

Moreover, energy-efficient task scheduling is essential for MPSoC designs in contemporary embedded systems [19]. We study this problem in Heterogeneous MPSoCs (HMPSoCs) based on NoC equipped with DVFS. Our energy-efficient task scheduling heuristic (ETSH) algorithm improves state-of-the-art methods by converting intra-data dependencies into inter-data dependencies represented by directed acyclic graphs (DAGs). Findings from synthetic and real-world task graphs (TGs) show that average energy efficiency can be as high as 38% and up to 20%, respectively, with and without coarse-grained software pipelining.

Smart industrial systems increasingly offer flexible processes incorporating human interactions with hard real-time operations, leading to varied task characteristics [18]. This is due to recent breakthroughs in IoT and cyber-physical systems. This paper suggests a novel task scheduling approach that uses two-phase scheduling and "virtual real-time tasks" to address this. Genetic algorithms are used in offline scheduling to identify processor voltage levels, memory locations, and to reserve virtual real-time jobs for interactive tasks. This helps to guarantee that hard real-time task deadlines are fulfilled. Interactive jobs are managed by online scheduling during the virtual real-time task periods. Offline scheduling should be updated periodically to account for changing interactive workloads. The experimental findings show an average energy consumption decrease of 66.8% without missing any deadlines and guaranteeing waiting times of less than three seconds for interactive jobs.

In order to satisfy the performance requirements of multimedia streaming applications, the use of MPSoCs based on NoC technology is expanding in contemporary embedded systems [16]. DVFS in conjunction with task-level coarse-grained software pipelining effectively reduces MPSoC energy

usage at the cost of extra delay. In this study, we present an energy-aware scheduler on heterogeneous NoC-MPSoCs based on voltage frequency island (VFI) for real-time streaming applications. We present R-CTG, a technique that outperforms R-DAG by integrating re-timing with DVFS to minimize latency without sacrificing energy efficiency. The experimental results show that our scheduler, ALI-EBAD, has a higher energy efficiency than competing task schedulers.

Furthermore, task mapping is essential for load balancing and communication optimization in multiprocessor sys-tem-on-a-chip software design. Compared to earlier approaches, the research [20] suggests an ILP-based strategy that takes into account both characteristics while using fewer variables. Additionally, it presents an enhanced ε-constraint method for flexibility and a task-processor-cluster strategy to boost scalability. The efficacy of the suggested strategy is authorized by experimental findings on a range of CPU systems.

Handling power consumption in real-time systems grants challenges, particularly concerning processing time for retrieving and monitoring voltage regulators' standards. While power gating has been discovered for power reduction, its effect on real-time capabilities remains unaddressed. Incorporating power-saving policies into RTOSs necessitates thorough attention to DVFS as well as clock gating, confirming an equilibrium between power optimization and real-time operational proficiency.

3. Problem Statement and its Proposed Solution

3.1 Problem Description

In multi-core systems with NoC designs, task deployment gifts significant complications to real-time performance, energy optimization, and system steadfastness. Multiple PEs operating in various power states are repeatedly used in these systems. Fault tolerance methods such as clock gating, task duplication, and DVFS are also mutual. The supervision of energy efficiency is made more challenging by the substantial energy expenditure associated with data processing and inter-PE communication. Vigorous power management familiarizes variability that compromises real-time performance and can affect erratic scheduling and neglected deadlines. Moreover, to avoid data loss and guarantee continuous operation, conserving system reliability obliges the use of effective fault management procedures, such as task redundancy and duplication.

3.2 Solution Framework

A comprehensive solution framework that syndicates cutting-edge task management approaches with energy-saving measures has been put forth to discourse these issues. In order to minimize energy consumption while meeting real-time restrictions, the framework practices a mixed-integer non-linear programming model for job allocation and scheduling. It takes into account computational requirements, task dependencies, and communication configurations. Utilizing DVFS, voltage, and frequency stages are vigorously adjusted to poise energy savings with performance essentials. Power usage is diminished during phases of inactivity with clock gating. Task duplication through multiple PEs advances reliability and guarantees that operations endure even in the event of hardware disasters. Besides, task scheduling effectiveness is increased by offloading it to a devoted hardware unit, and multipath data routing lessens NoC communication overhead. The framework's capacity to increase energy efficiency, real-time sensitivity, and system reliability is authenticated by experimental results.

4. Methodologies and Techniques

A multi-core system design is generated using the proposed methodology to look into ways to cut power usage without bargaining real-time performance. The system involves NoC with four compute units organized in a 2D-mesh topology and set in a master-slave formation, as shown in Figure 2. Expending an offloading strategy for every PE advances context switching and restraints real-time processes. While the principal PE is in control of voltage scaling, power supervision, and mapping techniques, each auxiliary PE is in custody of clock gating and frequency scaling. The hardware module that can be reconfigured is specified by the dotted outline.

One auxiliary way to increase system performance is to dispense task scheduling responsibilities to a co-processor. Exhausting a NoC topology, this scheme connects three slave PEs and one master PE to formulate a multi-core design. A voltage regulator is constructed into every slave PE to vigorously adjust voltage ranks to boost power output. Each slave PE also has a router attached to RTOS and a network interface processor (NIP) for task accomplishment.

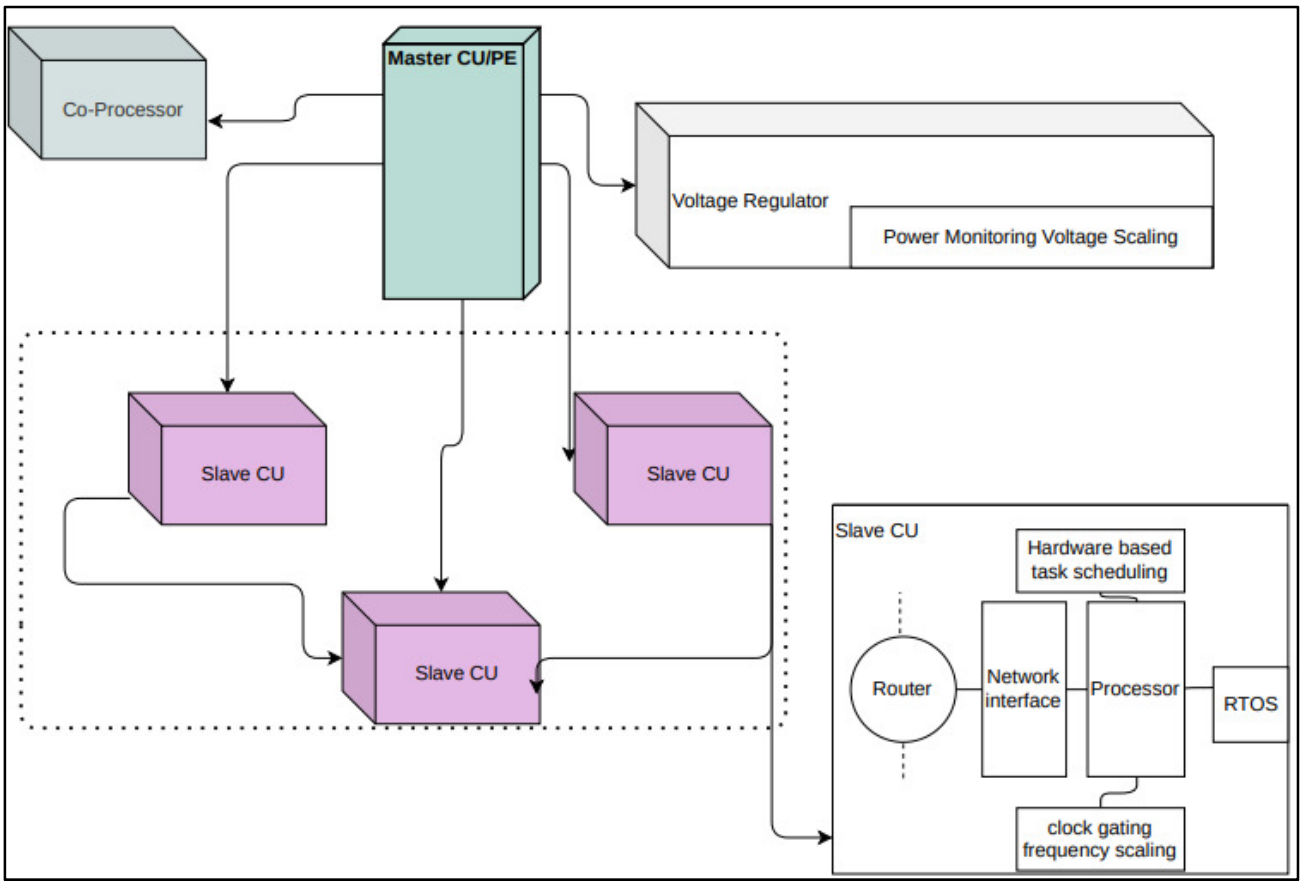

Fig. 2. Hardware structure comprising of a main processing element associated with NOC

The system strategy, power consumption checking, and task entrustment to the slave PEs are under the purview of the master PE. It is supplementary fixed to a co-processor, which knobs task scheduling, to expand system efficiency. The master PE is offloaded and latency is lessened by the co-processor, which is in control of scheduling mutually independent and dependent responsibilities.

In count, a job scheduling method is submitted for the master PE to enhance task distribution. With the assistance of this algorithm, which allocates jobs intelligently based on dependencies, communication configurations, and power measurements, the multi-core design's computing resources are utilized efficiently.

4.1 Algorithms

By allocating task scheduling obligations to a specialized co-processor, the co-processor task scheduling procedure benefits multi-core schemes activate more energy-efficiently. It also minimizes the interrelated power consumption and declines the processing liability on the primary PEs.

Algorithm 1. Co-processor task scheduling

```
Output: A task list L allocated to every slave PE
Input: Task list T with priorities for every task tj in T for each task tj in T do
if parent(tj)=heta, then
Add tj to the allocated task list L (master) for each slave PE do
Send tj to the coprocessor
End
return L
```

Every task in the prioritized task list is examined by the algorithm as it operates. The coprocessor is tasked with scheduling dependent tasks, whilst jobs without dependencies are assigned directly to the master PE. By shifting the scheduling responsibilities to the co-processor, the computational burden on the primary PEs is decreased and tasks can be assigned more effectively. Through task scheduling burden distribution to the co-processor, the primary PEs can reduce power consumption or even go into sleep mode.

In RTOS, Algorithm 2 optimizes task assignment in a multi-core system by considering both computation and communication energy. Primarily, it prepares the output parameters and nature tasks based on their enslavements and priority inside the RTOS. Then, it treasures PE with the lowest energy requirement, computes task assignment, implementation time, and communication parameters consequently. This algorithm guarantees efficient resource utilization and diminishes energy consumption in multi-core methods running RTOS.

Algorithm 2. Task scheduling algorithm

```
Input: yi and hi for all i in M0
Output: xik, uij, and tsi for all i in M0
initialize O[i]=−1 for all i in M0, sort tasks in M0 according to their dependencies and priority
for each task i in M0, where hi=1 do
Set MinEng to infinity for each PE k in N do
Calculate ecompk and ecommk using CalculateCompEnergy and CalculateCommEnergy Set
Eng to ecompk + ecommk if Eng < MinEng then
Set MinEng to Eng Set O[i] to k
end
Calculate xik according to O[i]=k, calculate uij and tsi according to xik, tcommi, and tcompi
using CalculateTaskCompletionTime and CalculateTaskStartTime
end
```

5. Conclusions

The NOC-based multicore design has publicized noteworthy achievements in system performance, latency fall, and energy efficiency with the accumulation of a co-processor for job scheduling. From side to side, the transfer of task scheduling obligations to the co-processor, the system proficiently condenses the overhead correlated to context switching and inter-processor communication. This causes execution configurations that are more expectable and established,

exclusively for real-time applications. This work contributed by designing a diverse multi-core architecture specifically tailored for real-time systems. It incorporated power-saving techniques and offloading methodologies, including a co-processor to optimize scheduling and reduce latency. Moreover, a task mapping strategy was introduced to efficiently allocate tasks to secondary computational units, taking into account task dependencies and power consumption metrics while ensuring real-time performance.

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